Remarks

Thorough examination by the Examiner is noted and appreciated. Examiner has indicated the most recent rejection is non-final.

The claims have been amended to clarify Applicants disclosed invention.

Support for the amendments is found in the original claims and the Specification.

No new matter has been added.

For example support for the amendments is found in the Specification at paragraph 0023:

"Referring to Figure 1D, in an important aspect of the invention, a remote plasma etch treatment including one or more inert plasma source gases such as nitrogen, helium, and argon is carried out to etch a portion of the barrier layer 20A. Preferably the remote plasma etch treatment is carried out to remove the barrier layer 20A covering the bottom portion 20B of via portion 18A of the dual damascene opening to reveal the underlying conductive portion 11, for example a copper interconnect. It has been found that the remote

plasma etch treatment carried out according to preferred embodiments, serves to make the barrier layer 20A more uniform in thickness at the sidewalls of the trench portion 18B and the via portion 18A of the dual damascene opening while removing the bottom portion of via portion 18A. Preferably, the barrier layer 20A following the remote plasma treatment is formed having a thickness between about 50 Angstroms and about 250 Angstroms."

Claim Objections

Examiner has objected to claim 6 requesting the removal of the word "comprises" in line 2. Applicants do not find such term in claim 6.

Claim Rejections under 35 USC 103(a)

1. Claims 1, 2, 6, 8, and 11 stand rejected under 35 USC Section 103(a) as being unpatentable over Chooi (USPUB 2002/0064941) in view of Ngo (US 6,525,428).

Chooi discloses a method of forming amorphous silicon spacers over trench and via sidewalls with an overlying metal nitride layer covering lining both the via and the trench (item 360 Figure 3F; item 460 Figure 4F) or with metal nitride spacers overlying the silicon spacers (along trench and via sidewalls)

(item 260, Figure 2F). In all three embodiments, the metal nitride is reacted with the underlying amorphous silicon to form a ternary metal silicon nitride liner (paragraphs 0018 and 0019). The ternary metal silicon nitride liner is taught to act as a fluorine trap, capturing fluorine from fluorinated dielectric layers and thereby protecting copper from fluorine attack (paragraph 0017 and 0048).

In all three embodiments, Chooi discloses an optional middle etch stop layer and teaches stopping on the etch stop layer when forming the trench, but teaches transferring the trench pattern into the etch stop layer following removal of the resist mask (paragraph 0047). In one embodiment, Chooi teaches etching through the metal nitride liner and barrier layer at the via bottom to expose a bottom conductor following formation of amorphous silicon spacers and overlying metal nitride liner (Figures 2D- 2F; paragraph 0050). In another embodiment the bottom of the via is etched to expose a bottom conductor **following formation of amorphous silicon spacers but before formation of the overlying metal nitride liner** (Figures 3D-3F; paragraph 0051). In a third embodiment, the bottom of the via is etched through the bottom barrier layer to expose a bottom

conductor **following formation of amorphous silicon spacers and metal nitride spacers** (Figures 4D-4F; paragraph 0053).

Ngo, on the other hand, discloses a dual damascene process including a graded middle etch stop layer formed of SiC/Si/Sic (see Abstract; col 3, lines 1-6). Ngo teach forming the trench opening to expose the Si layer in the middle etch stop layer as well as to exposing the bottom conductor in the via (col 5, lines 5 to col 6, line 2). A barrier layer (item 30, Figure 3) is then formed including covering a bottom via portion, followed by a seed layer (item 31, Figure 3), and followed by depositing a copper filling by electrodeposition (see col 6, lines 13-17).

There is no apparent motivation for combining the teachings of Chooi and Ngo. As pointed out, the method of Chooi is aimed at producing **terniary metal nitride spacers/liners** to prevent attack by fluorine from fluorinated dielectric layers on copper where the bottom conductor is **exposed prior to filling with copper** with the method of Ngo, which is taught to improve the adhesion of an overlying barrier layer, where the barrier layer **is deposited over the bottom conductor prior to filling with copper.**

Even assuming *arguendo*, a motivation for combining the teachings of Chooi and Ngo, such combination does not produce Applicants disclosed and claimed invention.

For example, the combination of Chooi or Ngo do not disclose a single etch process to improving a thickness uniformity along trench and via sidewalls as well as expose (reveal) the bottom conductor at the bottom of the via. Rather the process of Chooi could not be accomplished by a single etch process as Applicants disclose and claim. Chooi teaches the formation of **spacers** of either or both and amorphous silicon spacer and overlying nitride layer followed by a second etch process to expose the (reveal) the bottom conductor at the bottom of the (see Figures 2d-2f; 3d-3e; 4d-4f). Ngo does not teach or suggest removal of the barrier layer at the bottom of the via.

Moreover, nowhere do either Chooi or Ngo recognize the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A method for forming a copper dual damascene with improved

barrier layer thickness uniformity and improved electrical resistivity".

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

2. Claims 9 and 10 stand rejected under 35 USC Section 103(a) as being unpatentable over Chooi in view of Ngo, above, and further in view of Kim (US 6,436,303).

Applicants reiterate the comments made above with respect to Chooi and Ngo.

On the other hand, Kim teaches a remote plasma etching process to etch away undesired portions of dielectric films on a substrate including selectively removing films from peripheral surfaces (sidewall surface) while shielding major surfaces (horizontal surface) (see Abstract, col 1, lines 55-62), thereby **teaching away** from Applicants disclosed and claimed invention of

improving a barrier layer thickness uniformity along trench and via sidewalls **as well as removing the barrier layer at the bottom of the via (horizontal surface).**

Even assuming *arguendo* a proper motivation for combining the teachings of Chooi or Ngo with Kim, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

3. Claim 3 stands rejected under 35 USC Section 103(a) as being unpatentable over Chooi in view of Ngo, above, and further in

view of Smith (US 6,642,141).

Applicants reiterate the comments made above with respect to Chooi and Ngo.

The fact that Smith discloses the use of a graded silicon oxynitride film on a silicon nitride film as a **bottom etch stop** layer (items 150, 160; 180,190, Figure 3) (over a conductive portion) to improve adherence of an overlying fluorinated silicon oxide layer, does not help Examiner further in establishing a prima facie case of obviousness with respect to Applicants disclosed and claimed invention. For example, in the **trench first** process of Smith (form trench first, then the via) (see col 5, lines 6-14), Smith **does not** disclose or suggest the use of a **middle etch stop layer**, contrary to Examiners assertion, and such a middle etch stop layer would likely not be desirable or useful in the **trench first** dual damascene formation process of Smith (note that Applicants disclose and claim **formation of the via first, then the trench**). Moreover, the **bottom etch stop layer** of Smith is not disclosed or suggested to offer any benefit or advantage with respect to etching (bottom etch stop layer is **removed during via formation process**) see col 5, lines 10-26).

Even assuming *arguendo* a proper motivation for combining the teachings of Chooi or Ngo with Smith, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 4 and 5 stand rejected under 35 USC Section 103(a) as being unpatentable over Chooi in view of Ngo, above, and further in view of Wu (USPUB 2005/0110153).

Applicants reiterate the comments made above with respect to Chooi and Ngo.

On the other hand, Wu discloses a **bottom etch stop layer** (formed over a metal area; see item 16, Figures 1 and 2) and **does not disclose a middle etch stop layer**, contrary to Examiners

assertion, where the bottom etch stop layer is SiOC (paragraph 0027) or a composite of SiOC/and one or more of SiCN, SiCO, SiN, SiON, SiC, and SiO, preferably SiC/SiO (paragraphs 0030 and 0031) and offers the advantages of improving adhesion to copper and to an overlying low-K IMD layer (paragraph[0016] and which **prevents the bottom etch stop layer from being broken through during via etching** (paragraph 0032).

Thus, even assuming *arguendo*, a proper motivation for combining the teachings of Wu with Chooi and Ngo, such combination does not produce Applicants disclosed and claimed invention.

Double Patenting

6. Claims 1, 2, 6, 8, 11, and 12 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, and 12 of Tsai (US 6,878,615) in view of Ngo (US 6,525,428).

Statement of Common Ownership Pursuant to 35 USC 103(c)

Applicants attorney of record state that Tsai et al. (US 6,878,615) and Applicants instant application were, at the time the invention was made, owned by Taiwan Semiconductor Manufacturing Company.

Applicants respectfully point out that under a non-statutory obviousness type rejection, the disclosure of Tsai **is not to be used as prior art**, and a double patenting situation arises only where the **same subject matter** (identical invention) is **claimed** in Applicants patent and in Tsai. See MPEP Section 804 at page 800-22;

> When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, **the disclosure of the patent may not be used as prior art.**

and at page 800-30;

> **A prior art reference that renders claimed subject matter obvious under 35 U.S.C. 102(e)/103(a) does not create a double patenting situation where that subject matter is not claimed in the reference patent.** Where the subject matter that renders a claim obvious is **both claimed and disclosed** in a U.S. patent which satisfies the criteria of 35 U.S.C. 102(e), the examiner should make rejections based both on double patenting and 35 U.S.C. 103(a). For applications filed on or after November 29, 1999, rejections under 35 U.S.C. 102(e)/103(a) should not

> be made or maintained if the applicant provides evidence that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Applicants respectfully point out that the **same subject matter** as Applicants claimed invention **is not** claimed or disclosed in Tsai. It is clear that the process of Applicants claimed invention including claim 1, includes elements which are neither claimed nor disclosed in Tsai, and that Tsai includes elements disclosed and claimed which are not claimed by Applicants.

Tsai discloses and claims in claim 1, a process where a low-K protection lining is formed over the via following formation of a via in a via-first dual damascene formation process (see e.g., col 6, lines 30-35), forming a trench portion over the via, removing a portion of the low-K protection lining at the bottom of the via opening including a passivation layer, **and then forming a barrier layer over the low-K protection layer to line the dual damascene opening** (see claim 1).

Tsai neither claims not discloses "then forming an upper trench line portion extending through the upper dielectric

insulating layer thickness and partially through the middle etch stop layer;"

Or

"then removing a bottom portion of the barrier layer to reveal an underlying conductive area according to a plasma etching process, said plasma etching process further improving said barrier layer thickness uniformity along trench and via sidewalls; and,

then filling the dual damascene opening with copper to provide a substantially planar surface."

Applicants on the other hand, do not claim or disclose a low-K protection lining, removing a portion of the protective lining, forming a barrier layer on the protective lining, or forming a metal layer on the barrier layer, as claimed in claim 1 of Tsai.

As noted above, Ngo discloses forming a barrier layer but teaches leaving the barrier layer in place at the bottom of the via (as does Tsai) prior to filling with copper (see col 6, lines

13-29)

Even assuming *arguendo* a proper motivation for combining the references, such combination does not produce the claims of Applicants.

7. Claims 13, 16, and 18 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 10, and 12 of Tsai (US 6,878,615) in view of Ngo, above, and Kim.

Applicants reiterate the comments made above with respect to Tsai, Ngo, and Kim.

The fact that Kim teaches a remote plasma etching process to etch away undesired portions of dielectric films on a substrate including selectively removing films from peripheral surfaces (sidewall surface) while shielding major surfaces (horizontal surface) (see Abstract, col 1, lines 55-62) does not help Examiner in reproducing Applicants claims.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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